Back in 2015, only Outsourced Semiconductor Assembly and Test (OSAT) players were involved in Fan-Out (FO) packaging. In 2016, TSMC led the entry of foundries into this market with its integrated FO (iFO) packaging technology. Next, Integrated Device Manufacturers (IDMs) like Samsung joined the race with new in-house technology at the panel level. The result is that in 2019 OSATs have only a third of the market. Even with this reduced share, they are still developing and enhancing their portfolio in this segment. Recently ASE, in partnership with Deca Technologies, has entered the core market with its M-Series technology. Next, nepes bought the technology from Deca. As the market is continuously moving, System Plus Consulting offers an overview of the technologies on the market, providing the original equipment manufacturers’ (OEMs’) technical and cost choices of fan-out packaging.

This report provides insights on technology data for FO packaging for different application segments. It includes a comparative study of eight components from power management integrated circuits (PMICs) to processors to radar Monolithic Microwave Integrated Circuits (MMICs) using Fan-Out technology from different suppliers.

Physical data of several components has been compared in terms of process flow, cost and integration to provide a large panel of OEM technical and economic choices from the market such as:

- embedded Wafer Level Ball (eWLB) grid array from Infineon, Amkor and STATSChipPAC
- Redistributed Chip Package (RCP) from nepes
- M-Series from ASE/Deca Technologies
- Integrated Fan-Out (iFO) from TSMC
- Enhanced Panel Level Packaging (ePLP) from SEMCO

The report includes a description of each process flow for the five major fan-out technologies on the market. It also contains a complete cost analysis of the packaging and tries to explain OEM choices.
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7. TERMINATION

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