GaN-on-Sapphire HEMT Power IC by Power Integration

InnoSwitch3 Flyback Switcher Power IC in Anker PowerPort Atom PD 1

SP19480 - Power Semiconductor report by Amine ALLOUCHE
Laboratory Analysis by Nicolas RADUFE

July 2019 – SAMPLE
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<td></td>
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<td></td>
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<td>- Component Cost</td>
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©2019 by System Plus Consulting | GaN-on-Sapphire HEMT Power IC by Power Integrations
Executive Summary

The long-expected first GaN-on-Sapphire die has been integrated into a commercially-available device!

In this report, System Plus Consulting unveils Power Integrations’ technical choices from the device design up to the packaging.

The first GaN-on-Sapphire-based Power Integrated Circuit (IC) die has been found in the Wall-Charger PowerPort Atom PD1: A2017 from Anker. The die is co-packaged with three ICs constituting primary-side and secondary-side controllers in the SC1933C device.

To our great surprise, the power GaN HEMT was processed on a sapphire substrate which is a major breakthrough that we did not observe before in other power GaN HEMTs. The latter being generally processed on Silicon substrates.

In this report, System Plus Consulting presents a deep teardown analysis of the SC1933C. Detailed optical and Scanning Electron Microscope pictures and cross-sections with energy-dispersive X-ray analysis are included to reveal Power Integrations’ technical choices at the microscopic level of the IC and HEMT designs.

The report provides an estimation of the production costs of the ICs, the HEMT and the package as well as the estimated selling price of the component. Finally, the report includes a comparison with the GaN-on-silicon HEMT from Navitas. This comparison highlights the differences in GaN die designs and manufacturing costs.

A system-oriented analysis of the PowerPort Atom PD1: A2017 from Anker, can be found in our "GaN Chargers Comparison" report, which focuses on the impact of GaN die adoption in the latest wall charger designs and their performance.
GaN – Main Players Roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>1st Gen</th>
<th>2nd Gen</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td></td>
<td></td>
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<tr>
<td>2014</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2019</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Other companies are in R&D of GaN HEMT, but they are not included in this presentation.
Summary of the Physical Analysis

Package: (inSOP-24D)
- High creepage inSOP-24D Package.
- Dimensions: 10.9mm x 9.5mm x 1.6mm
- Number of Pins: xx pins
- Nb of dies: xx

- Dimension: xx mm²
- Electrical Connection:
- Placement in the package:

Die
- Dimension: xx mm²
- Electrical Connection:
- Placement in the package:
HEMT die Dimensions

- Die dimensions: \( xx \text{ mm}^2 (xxmm \times xxmm) \).
- The marking gives information about the mask set origin in xxx.
Die Process

- Pitch: \( xx \, \mu m \)
Die Cross-Section

- Die thickness: xx µm
- xx solder thickness: xx µm
Die Cross-Section – EDX Analysis: xxx

- The EDX analysis on the substrate xxx reveals the presence of a majoritary xxx (93.35%), proving a xxx of HEMT die.

<table>
<thead>
<tr>
<th>Element</th>
<th>P%</th>
<th>A%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xx</td>
<td>93.35</td>
<td>70.93</td>
</tr>
<tr>
<td>xx</td>
<td>2.11</td>
<td>2.73</td>
</tr>
</tbody>
</table>

Xxx thickness: xx µm

Die Cross-Section – SEM View
©2019 by System Plus Consulting
Die Cross-Section

- GaN: xx µm
- xx: xx µm
- Al: xx µm
- xx: xx µm
- xx: xx µm

Die Cross-Section – SEM View
©2019 by System Plus Consulting
Primary Side Controller IC “Die 1” – Delayering

IC Die – Optical View
©2019 by System Plus Consulting
Primary Side Controller IC “Die 1” – Delayering

- The process uses xx transistors.
- MOS transistor gate length: xx µm.
- We consider that the minimum dimension is xx µm.
Detailed Front-End Process – PowerCoSim+ Tool

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis

Manufacturing Process Flow
- HEMT Fab Unit
  - HEMT Process Flow
- ICs Fab Unit
  - ICs Process Flow
  - Component Packaging

Cost Analysis

Selling Price Analysis

Comparison

Related Reports

About System Plus
GaN Transistor - Process Flow (2/4)

xx for xx contact

- Xxx pattern and etching

SiN layer

- SiN deposition and patterning.

Xxx contact

- Xxx deposition and patterning.
Description of the Wafer Fabrication Unit – IC Die 1

- In our calculation, we simulate a production unit using 150mm wafers. IC manufacturing Process was simulated on ICPrice+ tool.

Estimated IC wafer fab unit:

- Name: xxx
- Wafer diameter: 150mm (6-inch)
- Capacity: xxx wafers / month
- Year of start: xxx
- Products: xxx
- Location: xxx

Excerpt from ICPrice+ tool
Secondary Side Controller IC “Die 4” – Front-End Summary

- The die area of the IC is xxx mm².
- The process is a xxx with xxx metal layers, xxx polysilicon layer with xxx.
- It is estimated that this process was introduced in xxx and requires xxx masking steps.

<table>
<thead>
<tr>
<th>Description</th>
<th>Name</th>
<th>Type</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC 4</td>
<td></td>
<td>Standard</td>
<td>(same as product)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Die characteristics</th>
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</thead>
<tbody>
<tr>
<td>Name</td>
</tr>
<tr>
<td>IC 4</td>
</tr>
<tr>
<td>Standard</td>
</tr>
<tr>
<td>(same as product)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Front-End description</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Material</td>
</tr>
<tr>
<td>Min. dimension</td>
</tr>
<tr>
<td>Start production</td>
</tr>
<tr>
<td>Si</td>
</tr>
<tr>
<td>Functions</td>
</tr>
<tr>
<td>Parameters</td>
</tr>
<tr>
<td>Device</td>
</tr>
<tr>
<td>Gate oxide nb</td>
</tr>
<tr>
<td>Polysilicon nb</td>
</tr>
<tr>
<td>Metal layers</td>
</tr>
<tr>
<td>Litho steps</td>
</tr>
</tbody>
</table>

Excerpt from ICPrice+ tool
### GaN HEMT Wafer Front-End Cost per Process Step

<table>
<thead>
<tr>
<th>Operation name</th>
<th>Step Cost (USD/Wafer)</th>
<th>Breakdown</th>
</tr>
</thead>
</table>

**Total** 100%
Primary Side Controller IC “Die 1” – Unprobed Wafer Cost

- The wafer cost is estimated between $xx and $xx according to yield hypothesis.

- The main part of the wafer cost is due to the xx with xx% and xx with xx%.
The die cost is estimated between $xx and $xx according to yield variations.

- Silicon cost accounts for xx% of the cost.
- The probe test, back grinding and dicing represent xx% of the cost.
- The scrap cost (xx%) is the total of all the losses during the back-end process.
### Estimated Selling Price

<table>
<thead>
<tr>
<th>Component Cost</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer Gross Profit</td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Component selling price</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Integrations</th>
<th>Gross Margin</th>
<th>51.6%</th>
</tr>
</thead>
</table>

- The component manufacturing cost ranges from $xx to $xx according to yield variations.

- The component selling price ranges from $xx to $xx according to yield variations.
## Comparison between Power Integrations and Navitas GaN HEMT dies

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Transistor</th>
<th>Package Type</th>
<th>Year</th>
<th>Die Size (mm²)</th>
<th>Lithography masks</th>
<th>Metal layers</th>
<th>Pitch (µm)</th>
<th>Epitaxy (µm)</th>
<th>Wafer thickness (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Integrations</td>
<td>SC1933C</td>
<td>SOIC</td>
<td>2018</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
</tr>
<tr>
<td>Navitas</td>
<td>NV6115</td>
<td>QFN 6-pin</td>
<td>2018</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
<td>xx</td>
</tr>
</tbody>
</table>

**Note:**
NV6115 component is a HEMT transistor with a driver interface. Detailed teardown of the Navitas NV6115 can be found in System Plus Consulting’s report “SP19464 - Navitas GaN HEMT 650V Family.”
Related Reports

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**POWER SEMICONDUCTORS & COMPOUND**
- GaN-Based Wall Charger Comparison 2019
- Navitas 650V GaNFast Power IC Family
- GaN-on-Silicon Transistor Comparison 2018
- Texas Instruments’ LMG5200 GaN Power Stage

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- Discrete Power Device Packaging: Materials Market and Technology Trends 2019
- Status of the Power Electronics Industry 2018
- Wireless Charging Technologies and Markets 2018
After long expectation, the first GaN-on-Sapphire die has been integrated in a commercially available device!

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**COMPLETE TEARDOWN WITH**

- Detailed optical and SEM photos
- Precise measurements
- Materials EDX analysis
- Supply chain evaluation
- Manufacturing cost analysis
- Estimated selling price
- Technology and cost comparisons with GaN-on-Si HEMT from Navitas.

The unique device with GaN-on-Sapphire technology in the Anker’s PowerPort Atom PD 1 wall charger.
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  - IC die cost
- Packaging Assembly Cost
- Component Cost
  - Back-end: Final test cost
  - Component cost

# Price Analysis
- Definition of Prices
- Estimation of Selling Price

## Price Analysis
- Technology and Cost Comparison Between Power Integrations and Navitas GaN HEMT Dies

# AUTHORS

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Tel: ......................................................................................
Email: ..................................................................................
Date: .....................................................................................
Signature: .............................................................................

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Last Name: .............................................................................
Email: ..................................................................................
Phone: ..................................................................................

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By credit card:
Number: |__|__|__|__|  |__|__|__|__|  |__|__|__|__|
|__|__|__|__|
Expiration date: |__|__|/|__|__|
Card Verification Value: |__|__|__|

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BIC code: CCFRFRPP
- In EUR
  Bank code: 30056 - Branch code: 00955 - Account: 09550003234
  IBAN: FR76 3005 6009 5509 5500 0323 439
- In USD
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