3D NAND FLASH MEMORIES

Comparison of Leading Edge 3D NAND Memories

TOSHIBA-SanDisk /SAMSUNG/SK HYNIX/INTEL- MICRON
Memory report by Belinda Dube
December 2018
# Table of Contents

## Overview / Introduction
- Executive Summary
- Reverse Costing Methodology

## Company Profile
- Toshiba/SanDisk
- Samsung
- SK Hynix
- Micron/Intel

## Technology & Market
- NAND Roadmap
- NAND Revenue

## Physical Analysis
- **Toshiba** Synthesis of the Physical Analysis
- **Toshiba** Physical Analysis Methodology
- **Toshiba** Physical analysis
  - Die
  - Cross-Section
- **Toshiba** Patents
- **Samsung** Synthesis of the Physical Analysis
- **Samsung** Physical Analysis Methodology
- **Samsung** Physical analysis
  - Die
  - Cross-Section
- **Samsung** Patents

## Manufacturing Process Flow
- Global Overview
- Wafer Fabrication Unit
- Front-End Process

## Cost Analysis
- Synthesis of the cost analysis
  - Yields Explanation & Hypotheses
  - NAND wafer and die cost
  - Front-End Cost
  - Component Cost

## Estimated Price and Manufacturer Gross Margin

## Company services
Executive Summary

The memory semiconductor industry continues to grow due to higher memory demand in consumer electronics and mass storage. Remarkable investments are channeled into the memory manufacturing business. IoT escalates this demand and hence manufacturers continue to increase the die density of memories at the same time aiming on reduction of the NAND die. The manufacturing process is complex compared to most semiconductor products. Each manufacturer proposes different manufacturing techniques with each generation in order to lower the wafer manufacturing by reducing the patterning count and cost.

This report details each process and features found in the latest NAND Memories. This full reverse costing study has been conducted to provide insight on technology data, detailed analysis of microstructural features, wafer manufacturing cost and die selling price of the latest LEADING EDGE 3D NAND MEMORIES produced by the four top manufacturers in the NAND memory industry.

Toshiba/SanDisk, Samsung, Micron/Intel have produced 64 Layers in their latest 3D NAND and SK Hynix have the highest number of layers in their NAND Memory having 72 layers in their latest 3D NAND.

Based on complete teardown analyses of the 3D, the reports provide the physical analysis and detailed manufacturing methods and cost estimation of each 3D NAND wafer. Comparison is made on the technology used, feature differences and the wafer fabrication technics used by each manufacturer and their estimated cost.

Moreover, the report proposes a comparison of the four different NAND memories, highlights the differences in design and manufacturing process.

All the 3D NAND memory manufacturers use the 12 inch wafer (300mm).
## Executive Summary

<table>
<thead>
<tr>
<th>Memory name &amp; Generation</th>
<th>Number of layers</th>
<th>Technology node</th>
<th>Package dimension</th>
<th>Number of dies in package</th>
<th>Die dimension</th>
<th>Flash Memory Area on die</th>
</tr>
</thead>
<tbody>
<tr>
<td>BICS3 Gen 3</td>
<td>64 layer TLC</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V-NAND Gen 4</td>
<td>64 layer TLC</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>pBiCS Gen 4</td>
<td>72 layer TLC</td>
<td></td>
<td></td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CuA Gen 4</td>
<td>64 layer TLC</td>
<td></td>
<td></td>
<td>8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Company Profile**

**Physical Analysis**

**Manufacturing Process Flow**

**Cost Analysis**

**Estimated Price Analysis**

**Related Reports**

**About System Plus**
Toshiba NAND- Packaging (with measurements)

- Length of memory:
- Length of package:
- Ratio of memory length to package:
- Length of Driver:
- Adhesive between two memories:
- Spacer between memory and driver:

Top memory die  Bottom memory die  Organic Spacer  Driver  PCB
Toshiba NAND - Multiple Layer Etch

Dielectric support pillar:

- High Aspect Ratio etching is performed through dielectric material oxide and alternating stack.

- The opening extending through the terrace is filled with SiO2.

- This support pillar is useful in providing mechanical support to the terrace structure to avoid collapse during SiN wet etching.

Channel Hole:

- High Aspect Ratio etch is also performed in creation, of channel hole and memory slits.
Transistor technology node: 620nm patterning is employed.
Samsung Memory - Memory Cross section - staircase

This technic uses one pattern to etch stairsteps. Each staircase comprises of...

The process is repeated times allowing layers to be exposed...

Etching technic:

- Samsung Patent is a that explains this technic
- This technic allows for Word Line exposure without an increase in lithography count.
- In the memory region each staircase comprises of layers.

Lithography count:
Word lines, selection gate lines have a staircase pattern to expose the WL in order to independently couple to contacts.
SK Hynix Memory - Effective unit Area

Total NAND Cell area:

Area of 4 strings =
Area of one string =

Memory density/die =
The memory density in active area =
Intel/Micron Memory - Double stack technic

Manufacturing Process Flow
Cost Analysis
Estimated Price Analysis
Related Reports
About System Plus

Double stack technic used by Micron/Intel:
- Stack 1
- Stack 2

Vertical Cell structure –SEM
©2018 by System Plus Consulting
## Die comparison

<table>
<thead>
<tr>
<th></th>
<th>Toshiba/SanDisk</th>
<th>Samsung</th>
<th>SK Hynix</th>
<th>Micron/Intel</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die size</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NAND Active Area</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Memory Die Area efficiency</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Die capacity</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Memory density/die</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Memory density/active area</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PGDPW/300mm wafer</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Potential GB/wafer</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Toshiba/SanDisk has the smallest die size. Toshiba/SanDisk is the only one that gains more memory space for less NAND, resulting in smaller dies and less costs. This results in more dies being produced per wafer, way higher than the other manufacturers, and they can produce a significantly higher number of dies and more GB are produced per wafer compared to the other manufacturers.
- Toshiba/SanDisk produces dies with the smallest NAND memory active area, effectively enhancing active area memory density.
- Toshiba/SanDisk has the denser die of 3.9 Gb/mm² followed by...
### Physical analysis summary

<table>
<thead>
<tr>
<th></th>
<th>Toshiba/SanDisk</th>
<th>Samsung</th>
<th>SK Hynix</th>
<th>Micron/Intel</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architecture</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Technology node</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Number of layers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Length of stacked layers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Full memory length</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Active Word layers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Alternating layers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Control gate layer</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Dielectric layer</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Cell gate type</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Storage type</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel hole length</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel hole trench width</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Slit Hole length</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Slit hole aspect ratio</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Support pillar length</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Physical analysis summary - staircase

#### Manufacturing Process Flow

1. **Cost Analysis**
2. **Estimated Price Analysis**
3. **Related Reports**
4. **About System Plus**

#### Table

<table>
<thead>
<tr>
<th></th>
<th>Toshiba/ SanDisk</th>
<th>Samsung</th>
<th>SK Hynix</th>
<th>Micron</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Staircase pattern</strong></td>
<td>stairs/pattern</td>
<td>stairs/pattern</td>
<td>stairs/pattern</td>
<td>stairs/pattern</td>
</tr>
<tr>
<td><strong>Word lines/stairstep</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Lithography count</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(advantage of...)
SK Hynix- Bit line contact and bit line

- Pattern and etch SiO2, deposition
- Pattern and etch SiO2, ALD bitline contacts

- Bit Line- CVD and CVD
- CVD SiO2, pattern and etch. CVD copper and CMP.

- CVD SiN protection layer.
- CVD SiO2 and Pattern wet etch Al.
- CVD SiO2. CVD passivation layers.
Intel/Micron – First deck: channel hole and slit formation

- Pattern and etch first deck
- CVD Silicon oxide, silicon nitride, silicon oxynitride

- Pattern and etch out
- CVD insulator layer
- CVD polysilicon and CVD
- Pattern and etch Slit hole, CVD
- CVD separation layers
The CMOS transistor and the metal layers front-end cost is 

The largest portion of the manufacturing cost is due to the 

at 38%
Memory 3D Front-End Cost

The **front-end cost** for the Memory is [specific cost value].

The largest portion of the manufacturing cost is due to the high yield at 60%.

Total Memory Front End Price includes the fabrication cost of CMOS transistor, the metal layers, the 64L memory and yield loss cost.

Total Memory Front End Price ranges from [specific range]. depending on the different yield loss.
By adding the probe test cost and the dicing, the wafer cost ranges from $ to $ according to yield variations.

The number of good dies per wafer is estimated to ranges from to according to yield variations, which results in a die cost ranging from $ to $.
Memory : Packaging Cost

Packaging includes 4 Memory Dies

The packaging cost is supposed to be done by a Intel and it is estimated at $_____ to $_____.

<table>
<thead>
<tr>
<th>Package Manufacturing</th>
<th>Nov-18</th>
<th>Feb-19</th>
<th>May-19</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Substrate / leadframe</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labour</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield loss Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Estimated Price Analysis

Related Reports

About System Plus

System Plus Consulting
Wafer Cost Comparison - Medium Yield

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>NAND Wafer Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toshiba</td>
<td></td>
</tr>
<tr>
<td>Samsung</td>
<td></td>
</tr>
<tr>
<td>SK Hynix</td>
<td></td>
</tr>
<tr>
<td>Intel</td>
<td></td>
</tr>
</tbody>
</table>

Wafer Cost Comparison - Medium Yield

Toshiba has the most expensive NAND Wafer fabrication cost, this is due to the higher yield loss during the NAND cell fabrication. Also, the cost per Gb is also higher.
Die Cost Comparison - Medium Yield

- 64 layer 64 mm²
- 64 layer 72 mm²
- 64 layer 64 mm²

Die cost is the least expensive to manufacture because of a die produced by compared to the other manufacturers.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Die Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toshiba</td>
<td>$</td>
</tr>
<tr>
<td>Samsung</td>
<td>$</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>$</td>
</tr>
<tr>
<td>Intel</td>
<td>$</td>
</tr>
</tbody>
</table>
The CMOS cost is because the transistor technology used is

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>CMOS Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toshiba</td>
<td>$</td>
</tr>
<tr>
<td>Samsung</td>
<td>$</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>$</td>
</tr>
<tr>
<td>Intel</td>
<td>$</td>
</tr>
</tbody>
</table>
Related Reports

- Toshiba-SanDisk 3D NAND Flash
- Emerging Non-Volatile Memory 2018
The ever-growing markets for consumer electronics and data centers are accelerating the demand for higher-capacity, reliable storage. This explains the impressive revenue growth in the memory industry from $77 billion to $177 billion between 2016 and 2018.

Manufacturers of flash memory that uses 3D NAND gates find it a challenge to meet this demand for higher storage capacity and reliability while lowering the cost per bit. Each manufacturer therefore implements different techniques. They change the storage type and memory cell design and stack more layers with each generation to increase bit density and reduce die sizes. The technological changes in the cell architecture and modification of the fundamental memory features add complexity to the manufacturing process. However, these techniques do lower the cost per gigabyte.

We present a technological and economical comparison of the latest generation of 3D NAND flash memory available on the market today from four different manufacturers. These are the 64-layer designs from Toshiba/SanDisk, Samsung and Intel/Micron and the 72-layer 3D NAND by SK Hynix. We base our analysis on full teardowns of the packages and the 3D NAND dies to unveil the technology choices used by the manufacturers.

We also identify the different participants in the supply chain. These two activities allow us to simulate the cost of the memory wafers and dies.

The report contains a detailed study of the latest NAND dies. The analysis also features a detailed study of die cross section and processes. The report details the physical analysis, highlighting the cell design and memory storage type. It matches the process description with the applicable patent. The report also includes the manufacturing cost analysis and estimation of the manufacturers Gross Margin.

Finally, it features an exhaustive comparison between the studied samples, highlighting the similarities and differences and their impact on cost.
TABLE OF CONTENTS

Overview/Introduction
- Executive Summary
- Reverse Costing Methodology
- Analysed Device Comparison

Company Profile
- Toshiba/SanDisk/Samsung/SK Hynix/Intel/Micron

Technology and Market
- NAND Roadmap
- NAND Revenue

Physical Analysis
- Toshiba/SanDisk
  - Overview
  - Die design
  - Cross-section
  - Patents
- Samsung
  - Overview
  - Die design
  - Cross-section
  - Patents

Manufacturing Process Flow
- Overview
- Wafer Fabrication Unit
- Front-End Process

Cost Analysis
- Summary of the Cost Analysis
- Yield Explanations and Hypotheses
- 3D NAND Wafer and Die Cost
  - Wafer front-end cost
  - Die cost
  - Component cost

Estimated Price and Gross Margin Analysis

AUTHORS

Belinda Dube is working for System Plus Consulting as Analyst in Semiconductor Memories and Integrated Circuits. She holds a Masters degree in Nano Science and Nanotechnologies from Ecole Central Lyon and INSA Lyon.

Véronique Le Troadec has joined System Plus Consulting as a laboratory engineer. Coming from Atmel Nantes, she has extensive knowledge in failure analysis of components and in deprocessing of integrated circuits.

RELATED REPORTS

Bluetooth 5: System-on-Chip Comparison 2018
A cost-oriented report on cutting edge components from NXP, Qualcomm, Dialog Semiconductor and Nordic Semiconductor, all dedicated to the fifth generation Bluetooth protocol. August 2018 - EUR 3,990*

Toshiba SanDisk 64 Layers 3D NAND Memory
The latest 3D NAND Flash memory produced by Toshiba and SanDisk for the iPhone X November 2018 - EUR 3,990*

NAND Service – Memory Research
NAND is expected to set another revenue record in 2018, before a flattish 2019. June 2018 - EUR 35,000*
COSTING TOOLS

Our analysis is performed with our costing tools IC Price+ and MEMS CoSim+.

System Plus Consulting offers powerful costing tools to evaluate the production cost and selling price from single chip to complex structures.

IC Price+
Performs the necessary cost simulation of any Integrated Circuit: ASICs, microcontrollers, DSP, memories, smartpower...

WHAT IS A REVERSE COSTING®?

Reverse Costing® is the process of disassembling a device (or a system) in order to identify its technology and calculate its manufacturing cost, using in-house models and tools.

CONTACTS

Headquarters
22, bd Benoni Goullin
Nantes Biotech
44200 Nantes
France
+33 2 40 18 09 16
sales@systemplus.fr

Europe Sales Office
Lizzie LEVENEZ
Frankfurt am Main
Germany
+49 151 23 54 41 82
llevenez@systemplus.fr

America Sales Office
Steve LAFERRIERE
Western USA
+1 310-600-8267
laferriere@yole.fr

Troy BLANCHETTE
Eastern USA
+1 704-859-0453
troy.blanchette@yole.fr

Asia Sales Office
Takashi ONOZAWA
Japan & Rest of Asia
+81-80-4371-4887
onozawa@yole.fr

Mavis WANG
Greater China
+86 979 336 809
wang@yole.fr

System Plus Consulting is specialized in the cost analysis of electronics from semiconductor devices to electronic systems. A complete range of services and costing tools to provide in-depth production cost studies and to estimate the objective selling price of a product is available.

Our services:
- STRUCTURE & PROCESS ANALYSES
- CUSTOM ANALYSES
- COSTING SERVICES
- COSTING TOOLS
- TRAININGS

www.systemplus.fr
sales@systemplus.fr
ORDER FORM

Please process my order for “Leading-edge 3D NAND Memory Comparison 2018” Reverse Costing® – Structure, Process & Cost Report
Ref: SP18422

☐ Full Structure, Process & Cost Report : EUR 4,990*
☐ Annual Subscription offers possible from 3 reports, including this report as the first of the year. Contact us for more information.

SHIP TO

Name (Mr/Ms/Dr/Pr): ..................................................................................
Job Title: .............................................................................................
Company: ...........................................................................................
Address: ................................................................................................
City: .............................................................. State: ..................................
Postcode/Zip: .....................................................................................
Country: ..............................................................................................
VAT ID Number for EU members: ....................................................
Tel: .................................................................................................
Email: ...............................................................................................
Date: .....................................................................................................
Signature: ........................................................................................

BILLING CONTACT

First Name: .......................................................................................
Last Name: .......................................................................................
Email: ...............................................................................................
Phone: ...............................................................................................

PAYMENT

By credit card:
Number: |__|__|__|__| |__|__|__|__| |__|__|__|__|
Expiration date: |__|__|/|__|__|
Card Verification Value: |__|__|__|

By bank transfer:
HSBC, 1 place de la Bourse, F-69002 Lyon, France
SWIFT or BIC code: CCFRFRPP
Bank code : 30056 - Branch code : 00170 - Account : 0170200156587
IBAN: FR76 3005 6001 7001 7020 0156 587

ANNUAL SUBSCRIPTIONS

Each year System Plus Consulting releases a comprehensive collection of new reverse engineering and costing analyses in various domains. You can choose to buy over 12 months a set of 3, 4, 5, 7, 10 or 15 Reverse Costing® reports.

Up to 47% discount!

More than 60 reports released each year on the following topics (considered for 2018):

• Power: GaN - IGBT - MOSFET - Si Diode - SiC
• Imaging: Camera - Spectrometer
• LED and Laser: UV LED – VCSEL - White/blue LED
• Packaging: 3D Packaging - Embedded - SIP - WLP
• Integrated Circuits: IPD – Memories – PMIC - SoC
• RF: FEM - Duplexer
• Systems: Automotive - Consumer - Energy - Telecom

*For price in dollars please use the day’s exchange rate
*All reports are delivered electronically in pdf format
*For French customer, add 20 % for VAT
*Our prices are subject to change. Please check our new releases and price changes on www.i-micronews.com. The present document is valid 6 months after its publishing date: December 2018

Return order by:
FAX: +33 (0)472 83 01 83
MAIL: YOLE DEVELOPPEMENT
75 Cours Emile Zola
69100 Villeurbanne – France

*For price in dollars please use the day’s exchange rate
*All reports are delivered electronically in pdf format
*For French customer, add 20 % for VAT
*Our prices are subject to change. Please check our new releases and price changes on www.i-micronews.com. The present document is valid 6 months after its publishing date: December 2018

METHODS DEVELOPMENT

ANNUAL SUBSCRIPTIONS

Each year System Plus Consulting releases a comprehensive collection of new reverse engineering and costing analyses in various domains. You can choose to buy over 12 months a set of 3, 4, 5, 7, 10 or 15 Reverse Costing® reports.

Up to 47% discount!

More than 60 reports released each year on the following topics (considered for 2018):

• Power: GaN - IGBT - MOSFET - Si Diode - SiC
• Imaging: Camera - Spectrometer
• LED and Laser: UV LED – VCSEL - White/blue LED
• Packaging: 3D Packaging - Embedded - SIP - WLP
• Integrated Circuits: IPD – Memories – PMIC - SoC
• RF: FEM - Duplexer
• Systems: Automotive - Consumer - Energy - Telecom

*For price in dollars please use the day’s exchange rate
*All reports are delivered electronically in pdf format
*For French customer, add 20 % for VAT
*Our prices are subject to change. Please check our new releases and price changes on www.i-micronews.com. The present document is valid 6 months after its publishing date: December 2018

METHODS DEVELOPMENT

ANNUAL SUBSCRIPTIONS

Each year System Plus Consulting releases a comprehensive collection of new reverse engineering and costing analyses in various domains. You can choose to buy over 12 months a set of 3, 4, 5, 7, 10 or 15 Reverse Costing® reports.

Up to 47% discount!

More than 60 reports released each year on the following topics (considered for 2018):

• Power: GaN - IGBT - MOSFET - Si Diode - SiC
• Imaging: Camera - Spectrometer
• LED and Laser: UV LED – VCSEL - White/blue LED
• Packaging: 3D Packaging - Embedded - SIP - WLP
• Integrated Circuits: IPD – Memories – PMIC - SoC
• RF: FEM - Duplexer
• Systems: Automotive - Consumer - Energy - Telecom

*For price in dollars please use the day’s exchange rate
*All reports are delivered electronically in pdf format
*For French customer, add 20 % for VAT
*Our prices are subject to change. Please check our new releases and price changes on www.i-micronews.com. The present document is valid 6 months after its publishing date: December 2018

METHODS DEVELOPMENT

ANNUAL SUBSCRIPTIONS

Each year System Plus Consulting releases a comprehensive collection of new reverse engineering and costing analyses in various domains. You can choose to buy over 12 months a set of 3, 4, 5, 7, 10 or 15 Reverse Costing® reports.

Up to 47% discount!

More than 60 reports released each year on the following topics (considered for 2018):

• Power: GaN - IGBT - MOSFET - Si Diode - SiC
• Imaging: Camera - Spectrometer
• LED and Laser: UV LED – VCSEL - White/blue LED
• Packaging: 3D Packaging - Embedded - SIP - WLP
• Integrated Circuits: IPD – Memories – PMIC - SoC
• RF: FEM - Duplexer
• Systems: Automotive - Consumer - Energy - Telecom

*For price in dollars please use the day’s exchange rate
*All reports are delivered electronically in pdf format
*For French customer, add 20 % for VAT
*Our prices are subject to change. Please check our new releases and price changes on www.i-micronews.com. The present document is valid 6 months after its publishing date: December 2018

METHODS DEVELOPMENT
Business Models Fields of Expertise

Custom Analyses
(>130 analyses per year)

Reports
(>40 reports per year)

Costing Tools

Trainings

About System Plus
- Company Services
- Contact

Company Profile
Technology and market
Physical Analysis
Manufacturing Process Flow
Cost Analysis
Estimated Price Analysis
Related Reports

Overview / Introduction

Company Services
Contact

Technology and market
Physical Analysis
Manufacturing Process Flow

Cost Analysis
Estimated Price Analysis
Related Reports

About System Plus
- Company Services
- Contact

Business Models Fields of Expertise

Custom Analyses
(>130 analyses per year)

Reports
(>40 reports per year)

Costing Tools

Trainings

About System Plus
- Company Services
- Contact

Overall / Introduction
Company Profile
Technology and market
Physical Analysis
Manufacturing Process Flow
Cost Analysis
Estimated Price Analysis
Related Reports
Contact

Headquarters
22 bd Benoni Goullin
44200 Nantes
FRANCE
+33 2 40 18 09 16
sales@systemplus.fr

Europe Sales Office
Lizzie LEVENEZ
Frankfurt am Main
GERMANY
+49 151 23 54 41 82
llevenez@systemplus.fr

America Sales Office
Steve LAFERRIERE
Phoenix, AZ
WESTERN US
T : +1 310 600 8267
laferriere@yole.fr

Troy Blanchette
EASTERN US
T : +1 704 859 0456
troy.blanchette@yole.fr

Asia Sales Office
Takashi ONOZAWA
Tokyo
JAPAN
T : +81 804 371 4887
onozawa@yole.fr

Mavis WANG
TAIWAN
T : +886 979 336 809
wang@yole.fr

www.systemplus.fr